Amendments to the Claims:

Please replace paragraph [0018] with the following amended paragraph:

[0018] FIG. 1A, is a cross-sectional view of an exemplary MIM capacitor 100 according to the present invention. In FIG. 1A, MIM capacitor 100 includes a bottom electrode 105 comprising a copper core conductor 110 and a conductive liner 115. MIM capacitor 100 further includes a conductive diffusion barrier 120 formed on a top surface 125 of bottom electrode 105, a dielectric layer 130 formed on a top surface 135 of conductive diffusion barrier 120 and an exemplary tri-layer top electrode 140 formed on a top surface 145 of MIM dielectric 130. Diffusion barrier 120 is intended to prevent copper diffusion out of bottom electrode 105 as well as prevent formation of CuO by reaction of copper core conductor 110 with MIM dielectric 130 when dielectric MIM 130 includes oxides. Top electrode 140 includes a core conductor 155, an optional bottom conductor 160 and an optional top conductor 165. While in FIG. 1A, conductive diffusion barrier 120 extends past sidewalls 150 of lower electrode 105 this feature does not occur in each and every embodiment of the present invention. The geometrical relationships between bottom electrodes [[105]], conductive diffusion barriers [[120]], MIM dielectrics [[130]] and top electrodes [[140]] are described *infra* in relationship to each of the various embodiments of the present invention.

Please replace paragraph [0025] with the following amended paragraph:

[0025] In FIG. 2D, an exemplary triple-layer conductor is deposited photo-lithographically patterned and RIE etched to form an exemplary tri-layer top electrode 238 on a

top surface 240 of MIM dielectric layer 236. Top electrode 238 is aligned over conductive diffusion barrier 232A and bottom electrode 226A. Top electrode 238 negatively overlaps (i.e. is smaller than) conductive diffusion barrier 232A. Top electrode materials and thicknesses have been described *supra*.

Please replace paragraph [0032] with the following amended paragraph:

[0032] In FIG. 4C, a MIM dielectric 336 and an exemplary tri-layer top electrode 338 (on a top surface 340 of the MIM dielectric) are formed by deposition of a MIM dielectric layer on top surface 334 of ILD 320 as well as over conductive diffusion barriers 326A and 326B, deposition of an exemplary triple layer conductive layer over a top surface of the MIM dielectric layer, photo-lithographically patterning a masking layer applied over the conductive layer to define the extent of MIM dielectric 336 and top electrode 338, performing an RIE of the MIM dielectric layer and the conductive layer, and removing the masking layer. Top electrode 338 is aligned over recessed conductive diffusion barrier 332A and bottom electrode 326A. Top electrode 338 positively overlaps (i.e. is larger than) recessed conductive diffusion barrier 332A. Conductive diffusion barrier materials and thicknesses, MIM dielectric materials and thicknesses and top electrode materials and thicknesses have been described *supra*.

Please replace paragraph [0038] with the following amended paragraph:

[0038] In FIG. 5C, an upper conductive diffusion barrier 435A, a resistor 435B, a MIM dielectric 436A and an exemplary tri-layer top electrode 438A1 (on a top surface 440 of the

MIM dielectric) and an exemplary tri-layer cap 438B are formed as follows: First, a second conductive diffusion barrier layer is deposited on top surface 434 of ILD 420 as well as over recessed conductive diffusion barriers 432A and 432B. Second, a MIM dielectric layer is deposited on top a surface of the second conductive diffusion barrier layer and an exemplary triple-layer conductive layer is deposited on a top surface of the second conductive diffusion barrier layer. Third, a masking layer applied over the conductive layer is photo-lithographically patterned to define the extent of MIM dielectric 436A, the extent of upper conductive diffusion barrier 435A and resistor 435B, and an initial extent of top electrode 438A1 and the extent of cap 438B. Fourth, an RIE of the MIM dielectric layer, second conductive diffusion barrier layer and the conductive layer is performed and the masking layer removed. Conductive diffusion barrier materials and thicknesses have been described *supra*.

Please replace paragraph [0045] with the following amended paragraph:

[0045] In FIG. 6D, first a MIM dielectric layer and then an exemplary triple layer conductive layer are deposited, photo-lithographically patterned and RIE etched to form an exemplary tri-layer top electrode 538 on a top surface 540 of a MIM dielectric 536. Top electrode 538 is aligned over conductive diffusion barrier 532A and bottom electrode 526A. Top electrode 538 positively overlaps (i.e. is larger than) conductive diffusion barrier 532A. Conductive diffusion barrier 532A positively overlaps (i.e. is larger than) lower electrode 526A. MIM dielectric materials and thicknesses and top electrode materials and thicknesses have been described *supra*.

Please replace paragraph [0052] with the following amended paragraph:

[0052] In FIG. 7D, a MIM dielectric 636A covering upper conductive diffusion barrier 635A, an exemplary tri-layer top electrode 638A covering MIM dielectric 636A and dielectric cap 636B covering resistor 635B and an exemplary tri-layer conductive cap 638B covering dielectric cap 636B are formed as follows: First, a MIM dielectric layer is deposited over upper conductive diffusion barrier 635A, resistor 635B, alignment mark 635C and exposed top surface 634 of ILD 620. Second, a masking layer is applied over MIM dielectric layer and photo-lithographically patterned to define the extent of MIM dielectrics 636A and 636B, an RIE of the MIM dielectric layer is performed and the masking layer removed. Third, an exemplary triple-layer conductive layer is deposited over MIM dielectrics 636A and 636B, alignment mark 635C and exposed top surface 634 of ILD 620. Fourth, a masking layer is applied over the conductive layer to define the extent of a top electrode 638A and a conductive cap 636B, an RIE of the conductive layer is performed and the masking layer removed. Top electrode 638 is aligned over MIM dielectric 636A and MIM dielectric is aligned over upper conductive diffusion barrier 635A and bottom electrode 626A. Top electrode 638A positively overlaps (i.e. is larger than) MIM dielectric 636A and MIM dielectric 636A positively overlaps (I.e. is larger than) upper conductive diffusion barrier 635A. MIM dielectric materials and thicknesses and top electrode materials and thicknesses have been described *supra*.

Amendments to the Claims:

Please amend claims 1, 2, 5, 14, 15, 18, 20 and 22-24. Please cancel claims 4, 6, 17 and 19. Please add new claims 31, 32, 33 and 34.

The claims are as follows:

Listing of Claims:

1. (Currently Amended) An electronic device, comprising:

an interlevel dielectric layer formed on a semiconductor substrate;

a copper bottom electrode formed in said interlevel dielectric layer, a top surface of said copper bottom electrode ~~co-planer with~~ recessed below a top surface of said interlevel dielectric layer;

a first conductive diffusion barrier formed on a top surface of said copper bottom electrode, a top surface of said first conductive diffusion barrier co-planar with said top surface of said interlevel dielectric layer;

a second conductive diffusion barrier in direct contact with said top surface of said ~~bottom electrode~~ first conductive diffusion barrier;

a MIM dielectric in direct contact with a top surface of said second conductive diffusion barrier; and

a top electrode in direct contact with a top surface of said MIM dielectric.

2. (Currently Amended) The electronic device of claim 1, wherein said second conductive diffusion barrier and said MIM dielectric both extend past at least two sides of said ~~bottom electrode~~ first conductive diffusion barrier.

3. (Withdrawn) The electronic device of claim 1, further including:

a dielectric diffusion barrier layer formed on said top surface of said interlevel dielectric layer; and

wherein said top surface of said conductive diffusion barrier is co-planer with a top surface of said dielectric diffusion barrier layer.

4. (Canceled)

5. (Currently Amended) The electronic device of claim[[4]] 1, wherein said ~~additional~~ first and second conductive diffusion barriers each independently comprise[[s]] about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations thereof.

6. (Canceled)

7. (Original) The electronic device of claim 1, wherein said MIM dielectric comprises about 2 to 20 nm of SiO_2, Si_3N_4 or SiC, a high K dielectric, Ta_2O_5, $BaTiO_3$, HfO_2, ZrO_2 or Al_2O_3, or combinations of layers thereof.

8. (Original) The electronic device of claim 1, wherein said top electrode comprises Al or W.

9. (Withdrawn) An electronic device, comprising:

an interlevel dielectric layer formed on a semiconductor substrate;

a copper bottom electrode formed in said interlevel dielectric layer;

a conductive diffusion barrier in direct contact with a top surface of said bottom electrode, said top surface of said bottom electrode recessed below a top surface of said interlevel dielectric layer, said top surface of said conductive diffusion barrier co-planer with said top surface of said interlevel dielectric layer;

a MIM dielectric in direct contact with a top surface of said conductive diffusion barrier; and

a top electrode in direct contact with a top surface of said MIM dielectric.

10. (Withdrawn) The electronic device of claim 9, wherein said said MIM dielectric both extend past at least two sides of said bottom electrode.

11. (Withdrawn) The electronic device of claim 9, wherein said conductive diffusion barrier comprises about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations thereof.

12. (Withdrawn) The electronic device of claim 9, wherein said MIM dielectric comprises about 2 to 20 nm of SiO_2, Si_3N_4 or SiC, a high K dielectric, Ta_2O_5, $BaTiO_3$, HfO_2, ZrO_2 or Al_2O_3, or combinations thereof.

13. (Withdrawn) The electronic device of claim 9, wherein said top electrode comprises Al or W.

14. (Currently Amended) A method of fabricating an electronic device, comprising:

(a) providing a semiconductor substrate

(b) forming an interlevel dielectric layer on said semiconductor substrate;

(c) forming a copper bottom electrode in said interlevel dielectric layer, a top surface of said copper bottom electrode ~~co-planer with~~ recessed below a top surface of said interlevel dielectric layer;

(d) forming a first conductive diffusion barrier in direct contact with said top surface of said copper bottom electrode, a top surface of said first conductive diffusion barrier co-planar with said top surface of said interlevel dielectric layer;

(e) forming a second conductive diffusion barrier on a top surface of said first conductive diffusion barrier;

[[(e)]] (f) forming a MIM dielectric in direct contact with a top surface of said second conductive diffusion barrier; and

[[(f)]] (g) forming a top electrode in direct contact with a top surface of said MIM dielectric.

15. (Currently Amended) The method of claim 14, wherein said second conductive diffusion barrier and said MIM dielectric both extend past at least two sides of said ~~bottom electrode~~ first conductive diffusion barrier.

16. (Withdrawn) The method of claim 14, further including:

(g) after step (c) forming a dielectric diffusion barrier layer on said top surface of said interlevel dielectric layer; and

wherein said top surface of said conductive diffusion barrier is co-planer with a top surface of said dielectric diffusion barrier layer.

17. (Canceled)

18. (Currently Amended) The method of claim [[17]] 14, , wherein said [~~additional~~] first and second conductive diffusion barriers each independently comprise[[s]] about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations thereof.

19. (Canceled)

20. (Currently Amended) The method of claim 14, wherein said MIM dielectric comprises about 2 to 20 nm of SiO_2, Si_3N_4 or SiC, a high K dielectric, Ta_2O_5, $BaTiO_3$, HfO_2, ZrO_2 or Al_2O_3, or combinations thereof.

21. (Original) The method of claim 14, wherein said top electrode comprises Al or W.

22. (Currently Amended) The method of claim 14, wherein:

step [[(d)]] (e) further ~~comprises~~ includes simultaneously forming a resistor ~~, an alignment mark or both a resistor and an alignment mark~~ on said top surface of said interlevel dielectric layer with said conductive diffusion barrier; and

step (f) further includes forming said MIM dielectric on a top surface of said resistor.

23. (Currently Amended) The method of claim 22, wherein said resistor ~~, said alignment mark or both said resistor and said alignment mark~~ comprises about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations of layers thereof.

24. (Currently Amended) The method of claim 14, further including [[(g)]] (h) after step [[(f)]] (g) depositing a reactive ion etch stop layer over all exposed surfaces of said second conductive diffusion barrier, said MIM dielectric, said resistor, said top electrode and said interlevel dielectric layer.

25. (Withdrawn) A method of fabricating an electronic device, comprising:

(a) providing a semiconductor substrate;

(b) forming an interlevel dielectric layer on said semiconductor substrate;

(c) forming a copper bottom electrode in said interlevel dielectric layer;

(d) forming a conductive diffusion barrier in direct contact with a top surface of said bottom electrode, said top surface of said bottom electrode recessed below a top surface of said interlevel dielectric layer, said top surface of said conductive diffusion barrier co-planer with said top surface of said interlevel dielectric;

(e) forming a MIM dielectric in direct contact with said top surface of said conductive diffusion barrier; and

(f) forming a top electrode in direct contact with a top surface of said MIM dielectric.

26. (Withdrawn) The method of claim 25, wherein said MIM dielectric both extend past at least two sides of said bottom electrode.

27. (Withdrawn) The method of claim 25, wherein said conductive diffusion barrier comprises about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations thereof.

28. (Withdrawn) The method of claim 25, wherein said MIM dielectric comprises about 2 to 20 nm of SiO_2, Si_3N_4 or SiC, a high K dielectric, Ta_2O_5, $BaTiO_3$, HfO_2, ZrO_2 or Al_2O_3, or combinations thereof.

29. (Withdrawn) The method of claim 25, wherein said top electrode comprises Al or W.

30. (Withdrawn) The method of claim 25, further including (g) after step (f) depositing a reactive ion etch layer over all exposed surfaces of said conductive diffusion barrier, said MIM dielectric and said interlevel dielectric layer.

31. (New) The electronic device of claim 1, further including a reactive ion etch stop layer over all exposed surfaces of said conductive diffusion barrier, said MIM dielectric, said interlevel dielectric, and said top electrode where said top electrode is not contacted by a conductor formed in a second interlevel dielectric layer formed over said first interlevel dielectric layer.

32. (New) The electronic device of claim 1, wherein at least two sides of said top electrode do not extend past said first conductive diffusion barrier.

33. (New) The method device of claim 14, further including after step (f), (g) forming a reactive ion etch stop layer over all exposed surfaces of said conductive diffusion barrier, said MIM dielectric, said interlevel dielectric, and said top electrode.

34. (New) The method of claim 14, wherein at least two sides of said top electrode do not extend past said first conductive diffusion barrier.

Amendments to the Drawings:

The attached sheets of drawings includes changes to FIGs. 4B. These sheets, which include FIGs. 2D, 2E, 2F, 4C, 4D, 4E, 5C, 5D, 5E, 5F, 6D, 6E, 6F, 7D, 7E and 7F, replaces the original sheets including FIGs. 2C, 2D, 2E, 2F, 4C, 4D, 4E, 5C, 5D, 5E, 5F, 6C, 6D, 6E, 6F, 7C, 7D, 7E and 7F. In FIGs. 2D-2F the lead on reference numeral 238 have been changed. In FIGs. 4C-4 E the lead on reference numerals 338 have been changed. In FIG. 5C the lead on reference numeral 438A1 has been changed. In FIGs. 5D-5F the lead on reference numerals 438A2 and 438B have been changed. In FIGs. 6D-6F the lead on reference numeral 538 has been changed. In FIGs. 2D-2F the lead on reference numerals 638A and 638 B have been changed.

Attachment: Replacement Sheets